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# Educating gate array designers

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**The immediate and future importance to industry of semi-custom integration particularly in gate array form is unquestioned. However, little attention has been given to the general training needs of designers exposed to this level of integration.**

**In this paper we present an educational programme for gate array designers that can form part of a formal graduate programme in engineering or serve as the basis for professional development (retraining) programmes. An important part of this programme is the implementation system that enables designs to be realized via a multi-project gate array wafer (MPGAW) approach.**

## 1. Introduction

The requirements of the electronic industry are increasingly toward a graduate population in electrical engineering that has a sound understanding of the various facets of microelectronics. These facets relate to the levels in integration of silicon technology and to circuit design. In particular with design, both full custom and semi-custom integration play an important role in the industry, and this must be reflected in any educational programme. Further any course must provide practical realization of the design in integrated form to enable testing to be undertaken and thus close the design loop. The former level of integration, namely full custom, is being covered in various educational establishments world-wide, following the Mead and Conway design methodology and implementation scheme[1]. However the latter area of semi-custom integration is generally not covered through the total cycle of circuit design, fabrication and testing. To rectify this situation at least within the undergraduate course leading to the degree of Bachelor of Electronic Engineering at the Royal Melbourne Insititute of Technology, an educational

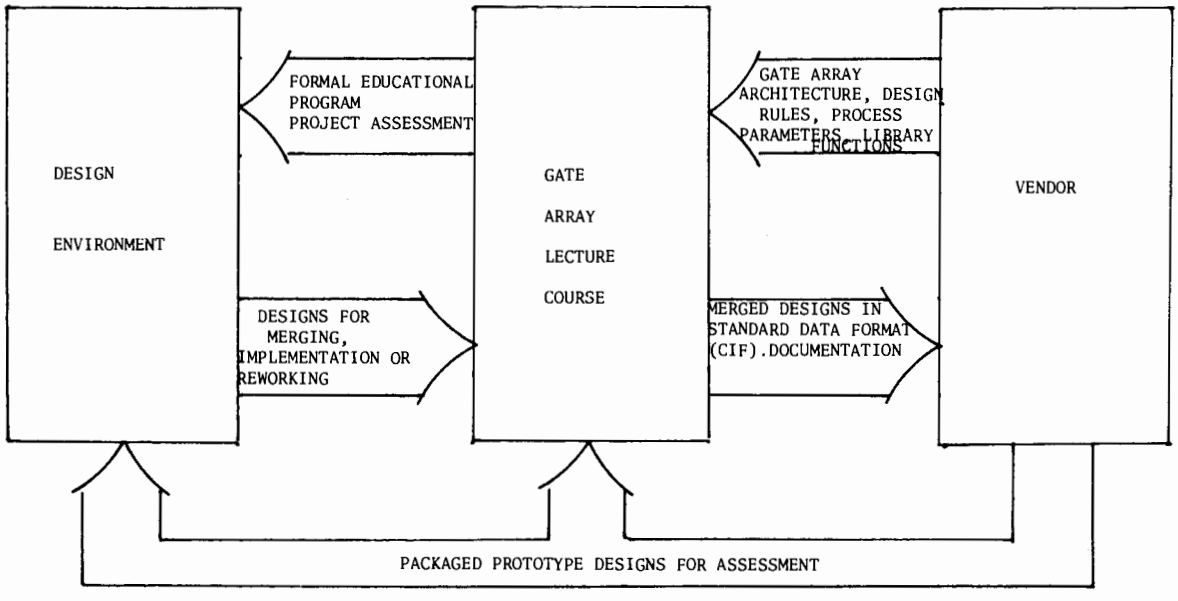


*Fig. 1 A schematic overview of the gate array educational programme.*

programme aimed at addressing this deficiency in the gate array area of semi-custom integration has been devised[2]. The programme relies on formal course work, together with a design and implementation system similar in concept to that of the Mead and Conway multi-project chip approach, however modified in this instance to produce a multi-project gate array wafer (MPGAW) as the vehicle for the hardware realization of designs. This programme has also been exercised in the retraining of practicing engineers by way of Professional Development Courses[3].

In Fig. 1 we depict schematically the various components that constitute the total educational programme[3]. The gate array course develops the methodologies for both analogue and digital design in various technologies. However, because the final designs are realized in single layer metal metal-gate complementary metal-oxide semiconductor (CMOS) technology, this technology is strongly emphasised. The course interfaces with the designers, design environment, and the vendor. In the latter case a clean interface has been developed which includes a flow of relevant production and design data from the vendor, and an implementation path back to the vendor. This facilitates rapid fabrication at a fraction of normal development costs, since many independent student designs are merged to form a unique mask to thence produce a multi-project gate array wafer (MPGAW). Finally, to close the loop, prototypes are returned after fabrication and packaging to the designers for assessment. Design, fabrication costs and turn around time to prototype level are therefore considerably reduced in comparison with conventional gate array prototyping, and also with custom design concepts such as multi-project chips (MPCs) or multi-project wafers (MPWs)[4]. In this paper we expand on the above points.

## 2. Lecture course and vendor considerations

The evolution of gate arrays has been such that for a particular application very often one technology is more suited than another[5]. For example we depict in Fig. 2 a decision matrix that reflects array technology to application. Obviously where high speed is of concern, such as CPU applications in the computer industry, the various forms of emitter-coupled-logic (ECL) would be an obvious choice at the expense of power dissipation and packaging density, these latter two points being complemented by the lower speed logics of CMOS and integrated injection logic ($I^2L$).

Consequently any course on semi-custom gate arrays must provide at least a general overview of technological considerations, involving a superficial consideration of device physics with sufficient depth to provide an understanding of speed and power limitations, design and layout considerations, cost, availability, second sourcing etc.

Whilst multi-layer interconnect structures are now common in industry[6], when considering gate array design at the undergraduate level single-layer metal single-mask systems of medium complexity provide sufficient understanding. This is particularly so when hand-routing of library macros serve as the basic layout tool. A single-layer metal two-mask process (metal and vias) considered by Hurst[7] is an attractive alternative when auto-routing and universal logic primitives are considered. Consequently during the course we concentrate our attention on single-layer metal gate array technologies, in particular CMOS, NMOS, integrated injection logic ($I^2L$) and common mode logic (CML). Detailed design and layout considerations, however, are only provided for the bipolar technolgy of $I^2L$ and that of metal-gate CMOS for MOS technology.

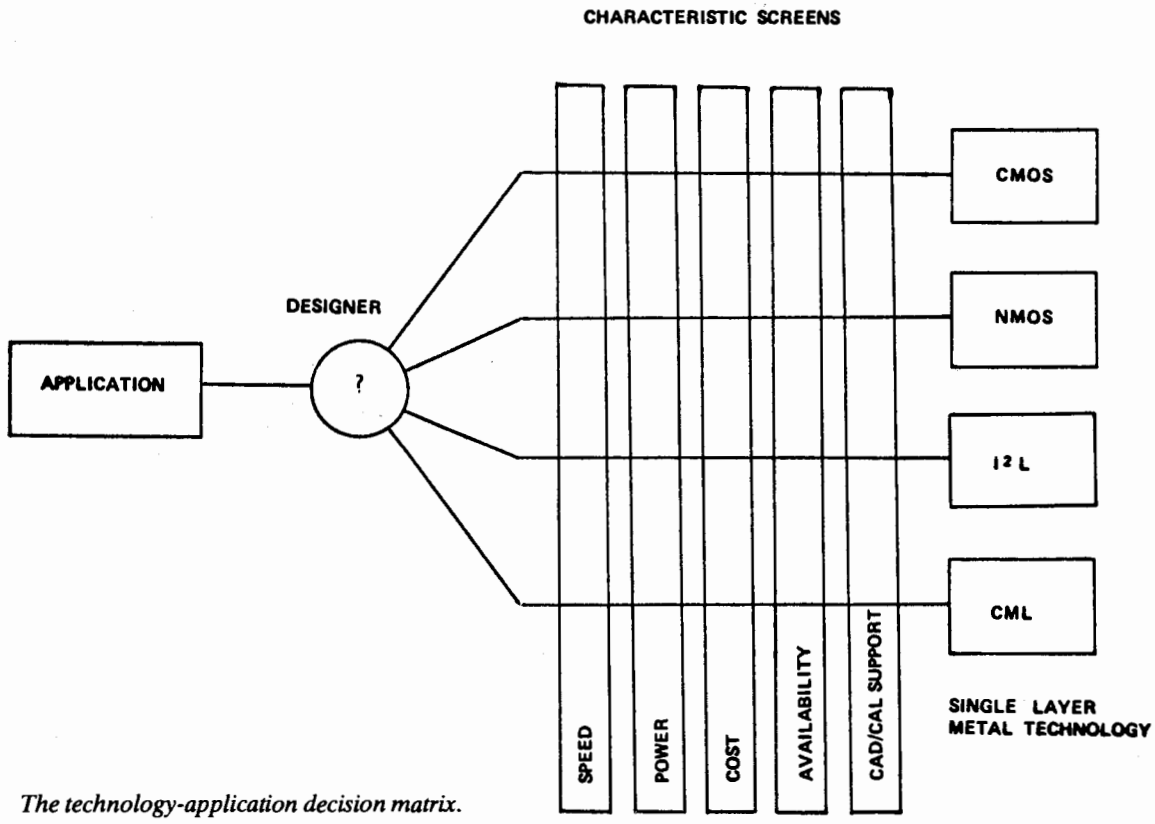


*Fig. 2 The technology-application decision matrix.*

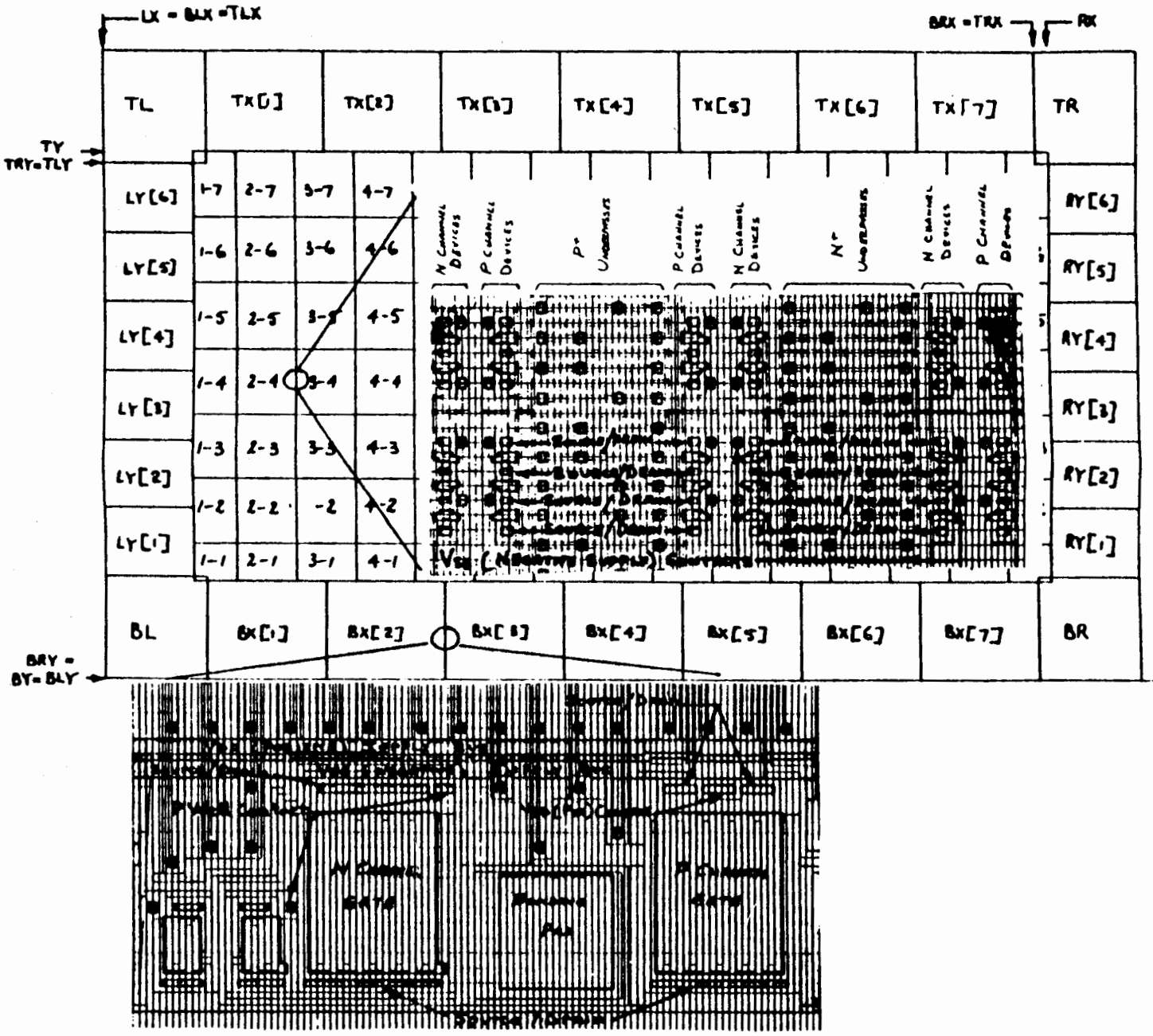


*Fig. 3 A schematic of the AWA 2600 gate array, with the appropriate student partitioning.*

For design implementation we concentrate on one technology and one array type within that technology. For convenience, the metal-gate CMOS array AWA 2600 is used, since it is a low complexity, well established, high yield, low cost array*. The AWA 2600 follows a somewhat standard layout for gate arrays. A complement of internal P and N channel devices capable of various logic function interconnections are interspersed between columns of $P^+$ and $N^+$ 'cross unders' in the internal cell array, see Fig. 3. Separate isolation wells are also provided to allow multiple on-chip supply voltages. With a two or three input NOR-NAND gate constituting a gate definition, the internal complexity of the AWA 2600 is set at a maximum of 200 gates. Various peripheral cells for input/output applications, such as high power and medium powers buffers, are interspersed between the 36 bonding pads. To facilitate single-layer metal interconnections the normally unused area-consuming guard ring diffusions provide 'built in' supply rails that are fed from a peripheral bus. Figure 3 shows an AWA 2600 gate array schematic, with the partitioning arrangements necessary to assist with the design process. The peripheral cells are identified by a top, bottom, left and right, X and Y identifier, whilst the internal array is subdivided on a matrix basis. All cell designs could thus be uniquely wired and replicated at any identical sites in the array. Also displayed is the grid line matrix for the 7.5$\mu$m metal interconnections. Column spacings of 6$\lambda$, of which every second line is available for adjacent metal, and a row spacing of 14$\lambda$ is used, where $\lambda = 1.25\mu$m. A considerable portion of the course is spent on the detail of this gate array from both a technological and a design point of view.

*AWA 2600 is a gate array produced by AWA Microelectronics, 348 Victoria Road, Rydalmere NSW Australia, who act as the vendor for our educational programme.

### 3. The design environment

At present the heart of the design environment is a number of microcomputer based workstations with graphics support via Visual 550, Tektronics 4010 and 4014 display terminals, and hard copy through Servogor 181 high resolution multi-colour plotters. Initially Z80A processors with 64K RAM and 8 inch DSDD floppy discs have been used. Recently acquired workstations incorporating 68000 based processors, 256K RAM and high resolution raster scan visual display units will augment the Z80A stations.

Design layout tools include BOXES, a Pascal-based geometric composition tool, CIFVAL, a Caltec Intermediate Form (CIF) validation program[1], and CIFPLT, a plotting program. The above programs are all available on the Z80A systems. Higher levels of layout and design verification are being installed on the 68000 workstations to provide design rule checking, electrical connectivity checking and circuit extraction.

Our main circuit simulation tool is SPICE 2F. However high levels of simulation are available using DIANA and LOGMOS, all installed on larger machines and mainly batch accessible.

Well characterised functional library macros based on the grid structure of Fig. 3, for example multiple-input Boolean gates, Exclusive-OR, Schmitts, etc., are provided, and their use encouraged. Designs are completed by final cell interconnect, and by taking appropriate action in 'tying off' excess gates and protection with I/O cells.

As in any design environment, group appraisal and design critique plays a significant and vital role. Sufficient provision for round table discussion and group interaction is provided and strongly encouraged.

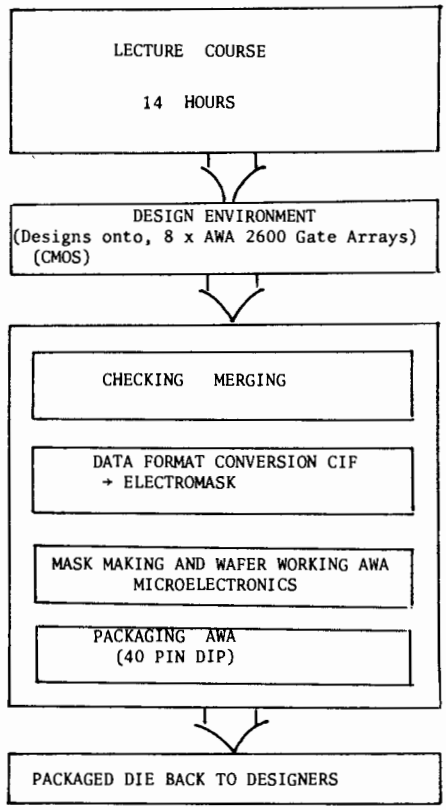


*Fig. 4 The MPGAW implementation system.*

### 4. The multi-project gate array wafer implementation system

A schematic flow chart is shown in Fig. 4 that provides detail on the implementation system used in this

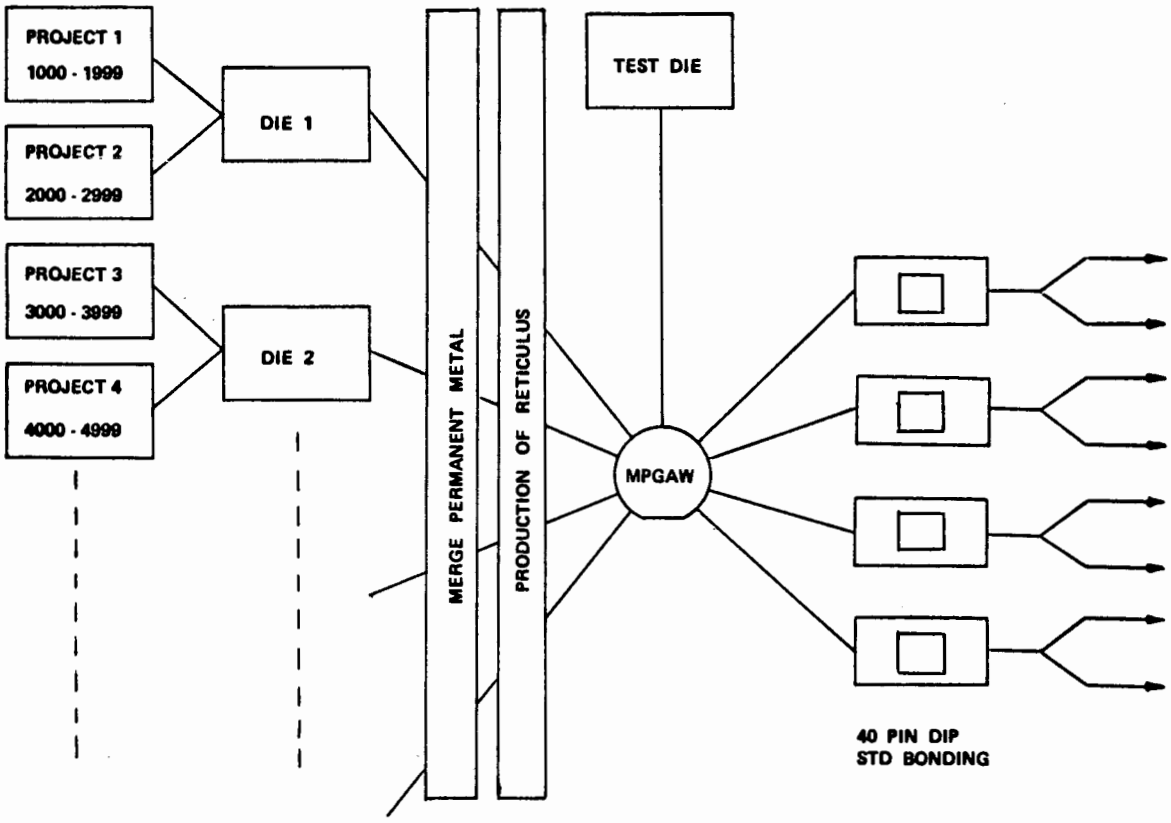


*Fig. 5 The merging and processing procedure.*

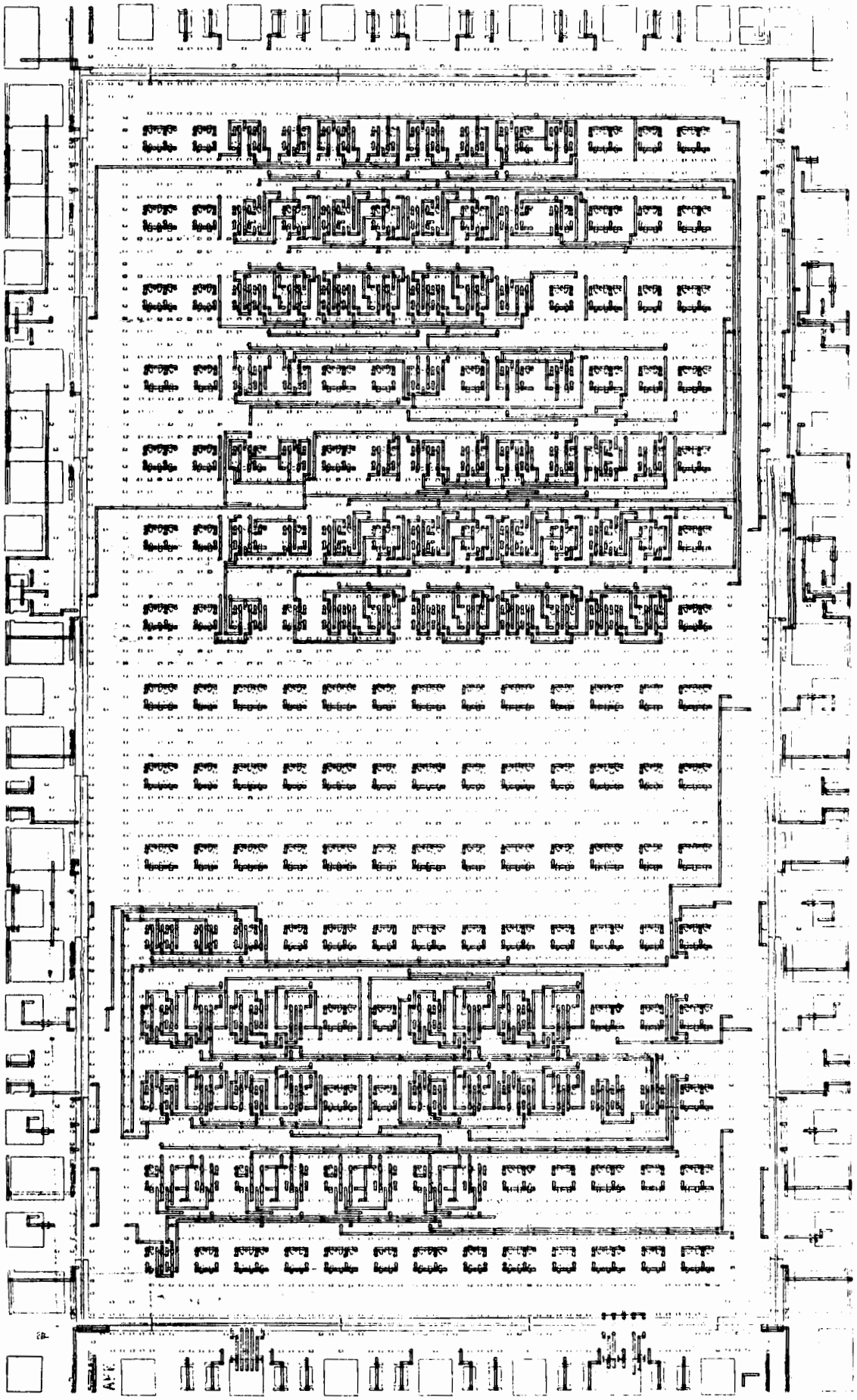

*Fig. 6 Layout of a shared AWA 2600 die.*

educational programme. Before the course students are encouraged to investigate a design of their own choice, or they are provided with a project that would constitute appropriate designs for their project work during the course. These projects are of moderate complexity and not more than ½ an AWA 2600 (approx 100 gates). We set a limit of a multiple of eight projects i.e. eight, sixteen, twenty-four etc. since projects share an array, and because of economics and die-per-wafer limitations (four per wafer plus a test reticule). This results in eight projects per wafer. Gate array chip sharing obviously requires project compatability to avoid undue interaction between participants. As an example Fig. 6 shows two projects that share the one gate array. It is obvious from this figure that the designs are not complex, which enables students to meet the necessary design and layout deadlines that are imposed in the implementation scheme of Fig. 4.

After checking, which includes layout integrity, circuit correctness, design rule violation, etc., an exercise that is invaluable and results in the detection of many catastrophic errors even for simple designs, merging is performed. An important and necessary step that we regard as part of the merging exercise is that of tying off unused gates, a step peculiar to CMOS gate array design.

The task of merging is reasonably simple and straight forward with gate arrays compared to the MPC approach[4]. As shown in Fig. 5 all design files are unique with a unique starting frame, and consequently merging consists of the production of one file per array and our files per wafer. Files are described and transported in CIF[1]. Four files per wafer are associated with the mask fabricated to produce the final gate array wafer. Because the AWA 2600 wafers are pre-processed up to final metallization, only one unique mask per wafer is required. To generate this final mask five separate reticules are produced, namely four die types (eight projects), and one test circuit. After fabrication, sawn and packaged wafers with all pads bonded are returned to the designers, as outlined in Figs. 4 and 5.

Test verification of designs is a necessary step in closing the educational loop. Consequently during the time that the chips are being fabricated, 2-3 weeks, students continue with formal course work and are encouraged to set up test procedures for chip function verification. The number of circuits that meet the initial design specification is exceptionally high, perhaps attributable to the unambitious designs, allied to the rigorous checking and the high yield process.

## 5. Conclusion

An educational programme has been developed that meets the training need for gate array designers. To provide low cost, quick turn-around to prototype stage a unique implementation system has been devised and implementated. The success of the programme can be gauged by its immediate acceptance by undergraduate students, and the enthusiastic response to the conduct of the professional development courses.

## 6. Acknowledgment

The authors acknowledge the support of the Joint Microelectronics Research Centre, and Austalian Government-sponsored Centre.

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## BOOK REVIEW

# Modular Series on Solid-State Devices

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The two authors, both of whom are from Purdue University, Indiana, share the authorship of these four texts, G. W. Neudeck being responsible for Volumes 1 and 4, and R. F. Pierrett for the two intermediate volumes.

The texts are written for persons who have already a reasonably good background of elementary physics and electrical engineering, but who have yet to study semiconductor principles and solid-state devices. They are therefore suitable for students on engineering degree courses, and practising engineers in industry who require to be informed on these matters. They are not, however, of sufficient detail for a device physicist or anyone intimately concerned with device design.

The authors' concept in splitting the material into relatively short separate volumes is extremely commendable. It avoids the massive tome on semiconductor physics and fabrication which one can find elsewhere, and allows the reader to confine his reading to specific areas with the minimum of inconvenience. As far as possible each volume is complete in itself, but material covered in, say, Volume 3 or Volume 4 would not be entirely meaningful without some basic knowledge from earlier volumes. Nevertheless, the later volumes do constitute valuable entities in their own right.

The authors have produced very readable texts, with sufficient depth of treatment for all but the specialist student. Descriptive device action is adequately supported by device physics, with extensive use of graphs and other figures. Microelectronics fabrication details, however, are not covered in any detail. A series of problems with answers at the end of the text are given in each volume, together with a short list of further reading. The latter could well have been made more comprehensive for readers who require a greater width and depth of treatment.

These books, therefore, may be particularly useful for electronic equipment engineers involved with semi-custom design to have on their bookshelves for back-up background reading. We look forward to further volumes in this series which maintain this compact limited bandwidth coverage per volume.

S. L. HURST