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Mansim - A Timing and Logic Simulation Tool

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This paper describes and evaluates an event-based timing and logic simulation tool developed in a co-operative program between the Royal Melbourne Institute of Technology and Nanjing Institute of Technology. The program is written in PASCAL and can be run on small 8-bit microprocessor based work stations.

I. INTRODUCTION

Simulation can be an effective tool for the analysis and design of digital integrated circuits [1]. It is important to differentiate between the different simulation levels, namely: circuit, such as SPICE2 [2]; mixed mode, such as DIANA [3]; logic, such as SALOGS [4]; timing, such as MOTIS-C [5].

MANSIM (Melbourne And Nanjing SIMulator) is an event-based gate level timing and logic simulator. Written in PASCAL, it can also incorporate higher level algorithmic described functional elements. The logic simulation ensures that the Boolean operations specified combine to achieve an expected system function while the timing simulation accounts for element delay, interconnect, driving and load effects on the system timing.

The rationale for the development of MANSIM is:

1. The need for an effective logic and timing simulator for use on microprocessor based work stations.
2. A program available to and suitable for use at Nanjing Institute of Technology.

II LOGIC MODEL

The characteristic of the logic description is that it makes an instantaneous transition of state determined by logic function but at a time controlled by the timing simulator. (Fig. 1.)

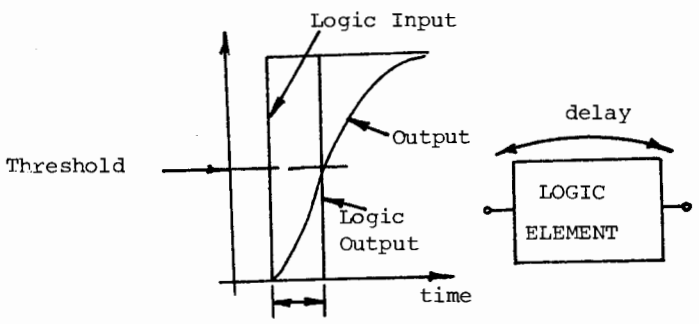

Fig. 1

As a gate level logic and timing simulator, MANSIM creates a number of primitive logic functions: Group 1. Logic gates: INVERT, AND, OR, NAND, NOR and Exclusive OR. Group 2. Unidirectional transmission gates: High level active unidirectional transmission gate and low level active unidirectional transmission gate. Group 3. Latches: High/Low level active D latch. Group 4. Flip-flops: Positive/negative edge active D flip-flop, positive/negative edge active T flip-flop, positive/negative edge active JK flip-flop, and master-slave JK flip-flop.

In addition user defined logic functions can be added by the insertion of appropriate PASCAL procedures and updating the element list.

III. TIMING MODEL

The timing model used in MANSIM is given in Fig. 2. It supports both high and low going delays within elements, inter-element propagation delay, as well as rise and fall time effects caused by source and sink capability in conjunction with connected loads.

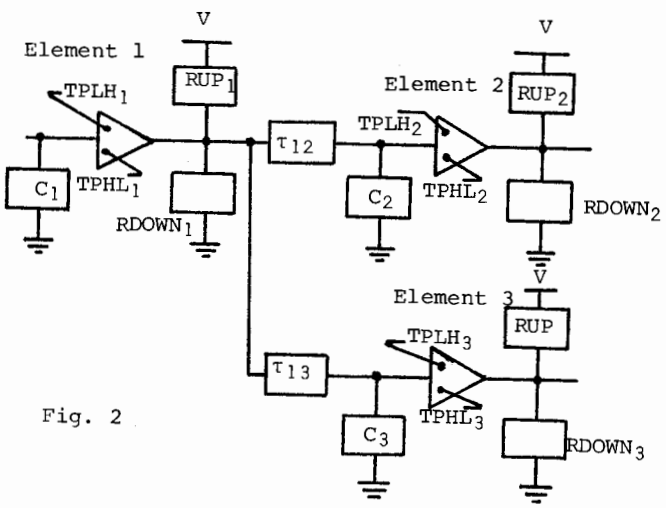

Fig. 2

The total delay from the output of an element (source) to the output of another element (load) consists of three parts. 1) Inter-element propagation delay τ. 2) The output resistance of the source-element (RUP or RDOWN) multiplied by the sum of input capacitances of all load-elements (C). When the output of the source-element changes from LOW to HIGH, RUP is used, while HIGH to LOW uses RDOWN. 3) Delay within the load-element (TPLH or TPHL - High/Low going delay). When the output of the load-element changes from LOW to HIGH, TPLH is used, while HIGH to LOW uses TPHL.

For example, when the output of element 1 changes from LOW to HIGH causing the output of element 2 to change from HIGH to LOW, the total delay from the output of the element 1 to the output of element 2 is

$$DELAY = \tau_{12} + RUP \cdot (C_2 + C_3) + TPHL_2$$

In use, a consistent set of R, C and time units are needed, for example, time in ns, R in K ohm, C in pf.

IV. FEATURES

1. GLITCHES

During the simulation, if a race exists in the circuit, then MANSIM will give a GLITCH warning with information, as to the time when the GLITCH occurs, the width of GLITCH, the source-element name and the destination-element name. This is helpful for the detection of timing errors.

2. SETUP-TIME AND HOLD-TIME ERRORS

For edge triggered flip-flops, MANSIM checks for SETUP-TIME and HOLD-TIME errors. The warning information given is the time when the error occurs, the deficiency, the source-element name and the destination-element name.

3. MULTIPLE OUTPUT

Facilities for describing multiple-output elements are provided which simplifies the input description of the circuits.

4. WIRED LOGIC

MANSIM is able to handle wired logic. If there are some elements whose outputs are connected to the same node in the circuit, MANSIM will recognize and indicate that there is a WIRED-AND, and give the corresponding result.

During the simulation if there is a WIRED-AND flagged at the outputs of certain elements by MANSIM and no WIRED-AND is intended, an error in the corresponding part of the description of the circuit is detected and can be corrected.

5. TRISTATE ELEMENT

MANSIM enables incorporation of tristate elements and employs the same mechanism as wired logic to recognise the existence of any elements whose outputs are connected to the same node. In this case, if there is a prefix "T" to the logic function description of the elements (e.g., TNAND, instead of NAND) a TRISTATE structure is indicated and only activated elements are used in simulation result.

V. RESULTS

A number of circuits have been simulated using versions of MANSIM on the RMIT CYBER 720 and 8-bit microprocessor work stations with 64k RAM and 1 Mb D.S.D.D. floppy disc. At this time work station simulated circuits are limited to 29 elements.

An example of a full adder with carry latch is shown in Fig. 3. indicating circuit timing problems.

By way of comparison circuits have been simulated by MANSIM on CYBER 720 and by LOGMOS on VAX 11/750. Results are indicated in Table 1.

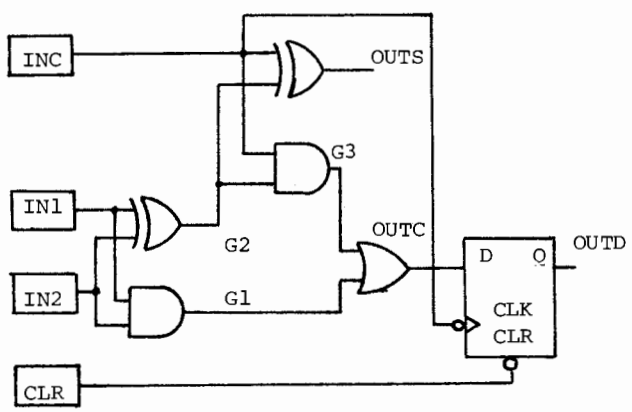

Fig. 3 (!≡0, >≡1)

CIRCUIT	COMPUTER TIME USED (SECS)		COMPUTER RESOURCE USED (K BYTES)	
	MANSIM	LOGMOS	MANSIM	LOGMOS
FULL ADDER (Fig. 3)	1.234	5.5	23.2	82.98
JK FLIP-FLOP (12 Elements)	1.745	6.1	23.2	83.44

TABLE 1

VI. CONCLUSION

Simulation is an important and proven technique in the design and specification of digital systems. In most cases programs to achieve this function reside on large computers. This paper has reported on a timing and logic simulation package capable of operation on an 8 bit microprocessor work station. The program includes a 3 part timing model, many standard logic functions, wired and tristate output capability and the ability to add algorithmically described elements.

VII. ACKNOWLEDGEMENTS

The authors wish to acknowledge the helpful discussion contributed by Mr. C. Fidge, Mr. A. Legrand, and Dr. P. Kennedy.

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