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Computer Aided Layout Aids for Custom and Semi-Custom Integrated Circuit Artwork

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A new teaching program introduces 150 students a year to the design of custom and semi-custom integrated circuits. The layout aids used in this program are supported by inexpensive 8-bit microprocessor based single-designer work-stations.

1 INTRODUCTION

All students in the Communication and Electronic Engineering Department at the Royal Melbourne Institute of Technology are introduced to semi-custom gate-array and full-custom circuit technologies in the third year of their four year undergraduate course; this material forms part of teaching programs in digital electronics and computing systems. These circuit technologies are then studied in greater depth in fourth year elective programs. The number of students exposed to this material is in excess of 150 each year.

The large numbers of prospective designers, the Departments equipment budget dictated that all design tools developed within the Department should be supported by inexpensive single-designer work-stations. Small electronics firms and firms attempting to introduce, or to gain experience with, these circuit technologies may have similar budgetary constraints. Our primary layout aids (BoxBld, Boxes, ABoxes, Router, CIFVal and CIFPlot) are written in Pascal and are all supported by microprocessor-based work-stations.

This paper describes the artwork layout aids currently being used at RMIT. It does not describe the simulation facilities which may be used in conjunction these aids. The tools are supported within the Department by 20 Z80A 8-bit microprocessor based work-stations each with 64Kbyte of RAM, 1 DS/DD 8" floppy drive, Tektronix 401x type displays, CP/M, Pascal(MT+) and network interface.

All work-stations within the Department are connected to an Ethernet-based local area network allowing ready transfer of information between stations and to the lithography facilities in the Departments Micro Electronics Technology Centre. This network is linked to other computing machinery and facilities external to the Department.

2 LAYOUT AIDS

The relationship of the layout aids described in the paper is shown in figure 1.

2.1 Leaf Cell Generation

In addition to the generation aids described in this section leaf-cells may be externally sourced, and PLA and finite state machine composition cells may be produced by the PLAGen program. The PLAGen program is written in Pascal and was distributed to participants in the CSIRO AusMPC'82 program.

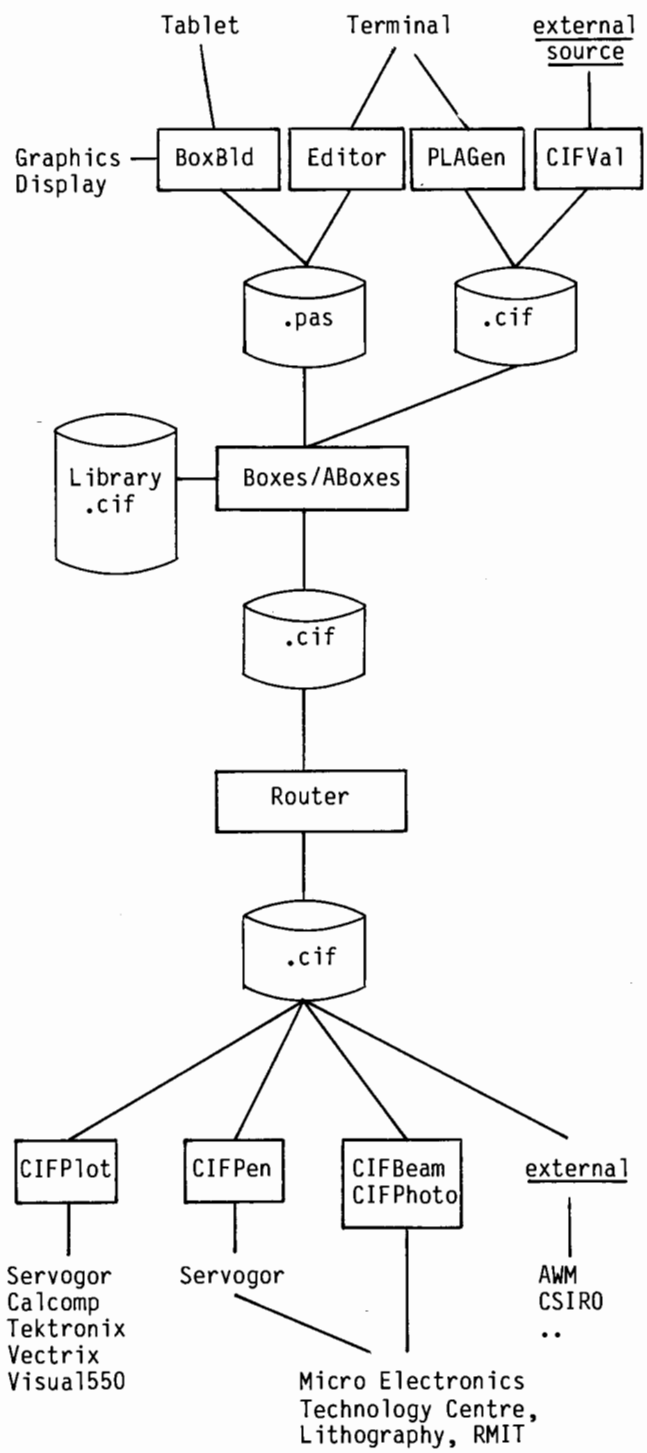

Figure 1 Layout and Lithography

2.1.1 BoxBld

BoxBld allows designers to digitise using a digitising tablet full-custom leaf-cells, gate-array metal or any other manhattan artwork; features are displayed as they are digitised. Some design rule checks are performed for the NMOS process and AWM 2600 gate-arrays. BoxBld generates Pascal procedures which describe the digitised structures. These procedures are compatible with the Boxes and ABoxes aids described below.

2.1.2 CIFVal

CIFVal checks externally sourced CIF leaf-cell description files for conformity to the published CIF language syntax. It performs some feature size layout rule checks for the NMOS process.

2.2 Composition Cell Generation

2.2.1 Boxes

Boxes is a layout language imbedded in the Pascal language. It is command compatible with the BELLE language distributed to participants in the CSIRO AusMPC'82 program. Boxes consists of procedures which are used to describe geometric symbols; these symbols may be iterated using Pascal control structures to generate repetitive geometries (RAMs, Adders etc.). Boxes generates an updated library of the users leaf and composition cells in addition to the CIF circuit description file. The circuit file may be augmented with net information for the Router.

2.2.2 ABoxes

ABoxes is a variant of Boxes tailored specifically for the AWM 2600 gate-array. Variable metal wires can only be placed on array wiring grid lines. The fact that the wiring grid for this array is 6 lambda in the x direction and 14 lambda in the y direction where lambda is 0.125 micron is concealed from the designer. ABoxes also updates the users library of leaf and composition (macro) cells in addition to generating the CIF circuit description file. The Router cannot wire AWM 2600 arrays.

2.3 Interconnection

2.3.1 Router

The Router accepts CIF files containing composition cells and net information. It then connects the cells using channel routing methods. It can route side channels and connect cells to pads. It generates CIF output. The Router may be used to interconnect leaf-cells to form composition cells.

2.4 Check Plots and Lithography

2.4.1 CIFPlot

CIFPlot generates check displays from CIF descriptions. Overlay files containing the permanent metal description of gate-arrays or grids may be displayed to aid checking. Symbols may be selected from the description file and displayed in isolation. Internal detail of symbols may be suppressed and only the bounding boxes displayed. CIFPlot supports Servogor, Calcomp, Vectrix colour display drivers and Tektronix 401x compatible display devices.

2.4.2 CIFPen

CIFPen produces positive penplot masks on Servogor plotters for 10:1 reduction to stripline and hybrid reticules.

2.4.3 CIFBeam and CIFPhoto

CIFBeam and CIFPhoto support the E-Beam and GCA lithography facilities in the Department's Micro Electronics Technology Centre.

3 CONCLUSIONS

The level of sophistication of the layout aids described is deliberately chosen not to isolate students from the target technologies. The use of these tools in their educational program is not an abstract exercise as the program also contain material in device fabrication and testing.

The aids have been used to produce a number of full-custom and semi-custom integrated circuit designs over the past two years. They are supported by inexpensive computing equipment and may be attractive to others attempting to gain experience with these technologies.

For more advanced circuit design the Department has access to current generation design tools and is actively developing next generation hierarchical design tools. Consistent with the philosophy adopted for our basic layout tools these tools are supported by M68000 based single-designer work-stations in a UNIX environment.

4 REFERENCES

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