VLSI PARC MELBOURNE '84

IREE, ROOM 212, 191 ROYAL PARADE, PARKVILLE, 3052

STAMP

VLSI PARC

VERY LARGE SCALE INTEGRATION

PACIFIC ASIAN REGION CONFERENCE

15th - 17th May 1984

SOUTHERN CROSS HOTEL
MELBOURNE
AUSTRALIA

ADVANCED PROGRAMME

Organised by:

Institution of Radio and Electronic Engineers Australia

Institute of Electrical and Electronic Engineers Inc.

Institution of Engineers, Australia

ADVANCE PROGRAMME

MONDAY, 14TH MAY

2.00 p.m. - 5.00 p.m. Visits (RMIT)

5.00 p.m. - 7.00 p.m. Registration and Drinks

TUESDAY, 15TH MAY

7.30 a.m. - 8.30 a.m. Registration

8.30 a.m. - 8.50 a.m. Official Opening

SESSION I:
(Chairman: Professor T. Cole, University of Sydney)

VLSI IN THE PACIFIC-ASIAN REGION

8.50 a.m. - 9.20 a.m. Systems in silicon: concept or reality?
(J. Tobias, AMI)

9.20 a.m. - 9.50 a.m. Trends and Developments of VLSI in Japan
(H. Mukai, NTT)

9.50 a.m. - 10.10 a.m. Custom I.C. experience from a users perspective
(P. Lundsman, Teletronics)

10.10 a.m. - 10.30 a.m. An image preprocessing chip for carcass identification in the meat industry
(B. K. Marlow, R. Kemp and D. C. Greager, DSIR-NZ)

10.30 a.m. - 11.00 a.m. Morning Tea

SESSION II:
(Chairman: Mr. P. Tassicker, Gerard Industries)

UNIVERSITY AND INDUSTRY

11.00 a.m. - 11.30 a.m. University/Industry Co-operation
(Viswanathan, UCLA)

11.30 a.m. - 11.50 a.m. Industry/University Co-operation in VLSI
(T. W. Cole, J. G. Rathmell, University of Sydney)

11.50 a.m. - 12.10 p.m. Product oriented teaching in the VLSI era
(J. Butcher, Middlesex Polytechnic)

TUESDAY, 15TH MAY (Cont.)

12.10 p.m. - 12.30 p.m. Design experience with the Dulmison 186ioc
(D. M. Gedye, G. R. Hellestrand and F. N. Yong, University of NSW)

12.30 p.m. - 2.00 p.m. Lunch

SESSION III:
(Chairman: Dr. D. G. Beanland, RMIT)

MICROELECTRONICS IN INDUSTRY

2.00 p.m. - 2.30 p.m. Is GaAs ready for VLSI
(R. Zuleeg, McDonnell Douglas)

2.30 p.m. - 3.00 p.m. Hybrids as an alternative technology
(W. Berryman, Hybrid Electronics)

3.00 p.m. - 3.20 p.m. Chart method to predict industrial success of proposed new VLSI-based products
(G. J. Fagan, Siemens)

3.20 p.m. - 3.50 p.m. Afternoon Tea

3.50 p.m. - 5.30 p.m. INDUSTRIAL PANEL SESSION
(Moderator: C. Meyer, AWA)

7.00 p.m. - 10.00 p.m. **RUMP SESSIONS**

WEDNESDAY, 16TH MAY

SESSION IV:
(Chairman: Dr. R. Potter, CSIRO)

VLSI STRUCTURES

8.30 a.m. - 9.00 a.m. Future trends of VLSI micro-processors
(H. Sazaki, NEC)

9.00 a.m. - 9.30 a.m. VLSI architecture and the mono-lithic nature of its technology
(J. C. Mudge, CSIRO)

9.30 a.m. - 9.50 a.m. A new CMOS VLSI architecture for signal processing
(K. Eshraghian, A. Dickinson, J. Rockliff, G. Zyner, R. Bogner, W. Cowley, B. Davis and D. Fensom, University of Adelaide)

9.50 a.m. - 10.10 a.m. How the world's largest I.C.'s were developed and produced
(NCM)

WEDNESDAY, 16TH MAY (Cont.)

10.10 a.m. - 10.30 a.m. On the evolution of semi-personalised integration
(H. B. Harrison and A. Legrand, RMIT)

10.30 a.m. - 11.00 a.m. Morning Tea

11.00 a.m. - 2.00 p.m. **SOAP BOX SESSION**

Selection
Of
Advanced
Papers
Based
On
X'cellence

A VLSI hardware breakpoint generator
(K. K. Wong and K. E. Forward, Monash University)

MANSIM – a timing and logic simulation tool (F. H. Payne, G. K. Egan and K. Y. Ding, RMIT)

Abstracted description and simulation of VLSI systems
(A. Dickinson and K. Eshraghian, University of Adelaide)

Overhead penalties in dynamically reconfigurable arrays of processing elements
(A. P. Clarke and W. Marwood, DRCS)

Fabrication of 2um length poly-crystalline silicon resistor having high resistance value
(Ming-Kwang Lee and Kun-Zen Cheng, ITRI-Taiwan)

Evaluation of super-buffer performance
(N. Ironmonger and M. Modra, University of Melbourne)

Experience with three phase clocking in multi-project experimental work
(K. M. Adams and S. Salom, University of Melbourne)

Stochastic modelling for profitable design of VLSI chips
(G. R. H. Bishop, University of Adelaide)

Wafer scale integration – a low cost common sense approach to VLSI
(J. Butcher, Middlesex Polytechnic)

(Continued . . .)

PROGRAMME (continued)

WEDNESDAY, 16TH MAY (Cont.)

Macro structures for silicon transistors
(K. Eshraghian, P. Evans and M. Pope, University of Adelaide)

Two designs of a two-four wire converter for applications in the telephone network
(H. B. Harrison and J. Royston, RMIT and A. Jennings, Telecom Research)

Studies in high density CMOS technologies
(K. Nannayakkara and G. Rigby, University of NSW)

CMOS array structures
(G. Smith, CSIRO)

SESSION V:
(Chairman: Dr. G. Hellestrand, University of NSW)

2.00 p.m. - 2.30 p.m. Aerospace requirements for VLSI
(H. Phillips, Aerospace Corp.)

DESIGN TOOLS

2.30 p.m. - 2.50 p.m. Basic computer aided layout aids for custom and semicustom integrated circuits
(G. K. Egan, F. H. Payne, A. Legrand and R. Allesio, RMIT)

2.50 p.m. - 3.10 p.m. An algorithm for the correct interconnection of VLSI-level macrocells
(C. Watson, CSIRO)

3.10 p.m. - 3.30 p.m. Automatic routing for VLSI circuits
(A. Legrand, RMIT)

3.30 p.m. - 4.00 p.m. Afternoon Tea

SESSION VI:
(Chairman: Professor G. Rigby, University of NSW)

4.00 p.m. - 4.30 p.m. Fine geometry devices
(G. Sai-Halasz, IBM)

TESTING

4.30 p.m. - 4.50 p.m. High reliability DC parameter measurement techniques
(T. Shimura, HP-Yokogawa)

WEDNESDAY, 16TH MAY (Cont.)

4.50 p.m. - 5.10 p.m. The detection of physical failures in VLSI chips
(P. Maxwell, University of NSW)

5.10 p.m. - 5.30 p.m. The use of marginal voltage analysis as a screening tool for ic reliability
(J. Thompson, Telecom Research)

7.00 p.m. - 11.00 p.m. **SPECIAL CONFERENCE FUNCTION**

THURSDAY, 17TH MAY

SESSION VII:
(Chairman: Dr. G. Price, Telecom Research Laboratories)

TECHNOLOGY

8.30 a.m. - 9.00 a.m. Advances in technology for VLSI fabrication
(T. Shibata, Toshiba)

9.00 a.m. - 9.20 a.m. Thermally nitrided Si02 (Nitroxide) for VLSI technology
(Chin-Tang Chen, Chun-Yen Chang, National Cheng Kung University and Chih-Hsiung Chen, Chuen-Nan Chen and Ming Kwang Lee ITRI, Taiwan)

9.20 a.m. - 9.40 a.m. VLSI interconnection: The emerging problem
(M. R. Haskard, A. M. Marriage and J. T. Bannigan, SAIT)

9.40 a.m. - 10.10 a.m. Technological implications of research developments in materials processing
(J. Williams, RMIT)

10.10 a.m. - 10.40 a.m. Morning Tea

SESSION VIII:
(Chairman: Dr. W. Berryman, Hybrid Electronics)

ANALOGUE DESIGN

10.40 a.m. - 11.10 a.m. Low voltage analogue MOS
(G. Rigby, University of NSW)

11.10 a.m. - 11.30 a.m. A library of analogue cells for the system designer
(M. R. Haskard and I. C. May SAIT)

THURSDAY, 17TH MAY (Cont.)

11.30 a.m. - 11.50 a.m. Charge transfer devices in nMOS
(P. Henderson, University of Sydney)

11.50 a.m. - 12.10 p.m. A tuneable CMOS switched capacitor filter
(G. A. Rigby, W. H. Holmes and C. K. Phuah, University of NSW)

12.10 p.m. - 12.30 p.m. The development of a custom LSI CMOS chip for a cohlear implant
(H. McDermott, University of Melbourne)

12.30 p.m. - 2.00 p.m. Lunch

SESSION IX:
(Chairman: Dr. C. Mudge, CSIRO)

2.00 p.m. - 2.20 p.m. VLSI at ISE — the design environment
(A. Dunn, University of Sydney)

2.20 p.m. - 2.40 p.m. An image processing computer
(P. Nickolls, University of Sydney)

2.40 p.m. - 3.00 p.m. Systollic back projection
(D. Skellern, University of Sydney)

3.00 p.m. - 3.20 p.m. A chip design for Chinese speech to text synthesis
(Ke-Cheng Zhou and T. W. Cole, University of Sydney)

3.20 p.m. - 3.30 p.m. Official Closing