Circuit Design
and Artwork Generation Tools

Dr. G.K. Egan
Digital Electronics and Computing Systems
February 1984

Department of Communication and Electronic Engineering
Royal Melbourne Institute of Technology

INTRODUCTION

For sufficient prospective circuit designers to have access, all design tools developed within the Communication and Electronic Engineering Department have been implemented on inexpensive single-designer engineering work stations. This is consistent with education budgets and the budgets of many small industries. Our primary design tools (BoxBld, Boxes, Router, CIFVal and CIFPlot) are all supported by Z80 8-bit microprocessor-based systems. Reflecting decreasing equipment costs, our next generation of hierarchical tools will be based on 16/32-bit microprocessor based stations in a UNIX environment. The current tools have been used successfully to produce a number of full-custom and semi-custom integrated circuit designs over the past two years.

This document catalogues all circuit design aids currently being used at RMIT. The tools are supported within the Department by the following computing machinery:

20 Z80A 8-bit microprocessor based stations each with 64Kbyte of RAM, 1 DS/DD 8" floppy drive, Tektronix displays (8), CP/M, Pascal(MT+) and network interface.

4 M68000 16/32-bit microprocessor based stations with 0.5Mbyte of RAM, 40Mbyte of winchester disk, 1 DS/DD 8" floppy drive, medium resolution colour graphics, mouse pointing device, UNIX, C, Pascal and FORTRAN and network interface.

2 A2 multi-pen plotters.

1 A0 digitising tablet.

The Department also has access to:

1 CDC Cyber, NOS, Pascal, FORTRAN.

1 DEC VAX 11/750, VMS, Pascal, FORTRAN.

1 DEC VAX 11/780, UNIX, C (UNSW).

All computing machinery within the Department is connected to an Ethernet-based local area network. This network is in turn linked to other machinery external to the Department.

LAYOUT TOOLS

The CIF or Caltech Intermediate Form referred to in this document is an internationally recognised low level artwork description language.

Leaf and Composition Cell Generation

Name: BoxBld

Origin: Digital Electronics and Computing Systems RMIT.
Language: Pascal
Machines: Z80 64Kbyte, DS/DD Floppy Drive, Tektronix Display, CP/M.
M68000, 0.5Mbyte, 40Mbyte Winchester, Tektronix Display, UNIX.

BoxBld allows designers to digitise using a digitising tablet full-custom leaf-cells, gate-array metal or any other manhattan artwork; features are displayed as they are digitised. Some design rule checks are performed for the NMOS process and AWM 2600 gate-arrays. It generates Pascal procedures which describe the digitised structures. These procedures are compatable with the Boxes aid described below.

Name: KIC II

Origin: Berkeley
Language: C
Machines: M68000, 1.0Mbyte, 40Mbyte Winchester, Colour Display, UNIX.
DEC VAX 11/7xx, UNIX.

KIC II is an interactive graphics editor for generating integrated circuit artwork. The output from KIC is translated to CIF.

Name: CAGL (Computer Aided Graphics Layout)

Origin: RMIT.
Machine: CAGL is a dedicated Layout engine based on Data General Nova Computers.

CAGL is a very high speed layout engine using special purpose hardware extensively. Its main use is for hybrid, stripline and pcb layout but it may be used for leaf and composition cell generation. The CAGL display files are translated to CIF.

Name: Boxes

Origin: Digital Electronics and Computing Systems, RMIT.
Machines: Z80 as above.
M68000 as above.
CDC Cyber.

Boxes is layout language imbedded in the Pascal language. It is command compatable with the BELLE language distributed by the CSIRO VLSI program. Boxes provides procedures allowing layer, feature, and geometric symbol specification; symbols may be iterated using standard Pascal control structures to generate repetitive structures (RAMs, Adders etc.). Symbols or leaf-cells

generated by BoxBld are compatable with Boxes.

Name: ABoxes

Origin: Digital Electronics and Computing Systems, RMIT.
Language: Pascal.
Machines: Z80 as above.
M6800 as above.
CDC Cyber.

ABoxes is a variant of Boxes tailored specifically for the AWM 2600 gate-array.

Synthesis

Name: PLAGen

Origin: -
Language: Pascal
Machines: Z80 as above.
CDC Cyber.

PLAGen is an NMOS process PLA or Finite State Machine composition-cell generator.

Name: SWINE

Origin: Digital Electronics and Computing Systems, RMIT.
Language: Pascal
Machines: CDC Cyber.

SWINE is a combinational logic reduction program.

Interconnection

Name: Router

Origin: Digital Electronics and Computing Systems, RMIT.
Language: Pascal.
Machines: M68000 as above.
CDC Cyber.

The Router accepts CIF files that contain composition cells and are augmented with netlist information. It connects the composition cells using channel routing methods. It can route side channels and connect cells to pads. It generates CIF output. The Router may be used at the composition cell level.

Name: DASOFT Printed Circuit Board Package

Origin: DASOFT
Language: Z80 Assembler.
Machines: Z80 as above.

The DASOFT is a documentation and routing package for printed circuit boards.

Artwork Validation

Name: Berkeley Tools

Origin: Berkeley
Language: C
Machines: M68000 as above.
DEC VAX 11/7xx, UNIX.

The Department has access to the set of aids collectively known as the Berkeley Tools. A subset of these tools are installed on our M68000 based engineering workstations. The tools provide design rule checking, circuit extraction, electrical rule checking and simulation from CIF artwork description files. The distribution of key tools in this set is restricted.

Name: CIFVal

Origin: Digital Electronics and Computing Systems, RMIT.
Language: Pascal.
Machines: Z80 as above.
M68000 as above.
CDC Cyber.

CIFVal checks externally sourced CIF files for conformance to the published CIF language syntax. It performs some feature size design rule checks for the NMOS process.

Name: CIFPlot

Origin: Digital Electronics and Computing Systems, RMIT.
Language: Pascal.
Machines: Z80 as above.
M68000 as above.
CDC Cyber.

CIFPlot generates check plots from CIF descriptions. It supports Servogor, Calcomp, Vectrix colour display drivers and Tektronix 401x compatable display devices.

Lithography

Name: CIFPen

Origin: Digital Electronics and Computing Systems, RMIT.
Language: Pascal
Machines: Z80 as above.

CIFPen produces positive penplot masks on Servogor plotters for 10:1 reduction to stripline and hybrid reticules.

Name: CIFEBeam, CIFPhoto

Origin: Digital Electronics and Computing Systems, RMIT.
Langauge: Pascal
Machines: Z8Ø as above.

CIFBeam and CIFPhoto are being developed to support the E-Beam and GCA lithography facilities in the Micro Electronics Technology Centre within the Department.

SIMULATION TOOLS

Name: Spice

Origin: Berkeley
Language: FORTRAN
Machines: CDC Cyber.

Spice is general analog circuit simulator which performs transient, DC and non-linear analysis. It is used for characterisation of sub-circuits or leaf-cells.

Name: ANOY
Origin: -
Language: FORTRAN
Machine: CDC Cyber.

ANOY is a general analog circuit simulator for small signal, linear ac analysis. It also calculates component sensitivity.

Name: Diana

Origin: Leuven
Language: MORTRAN (object code)
Machines: DEC VAX 11/7xx, VMS.

Diana is a mixed mode circuit simulator and is used for larger sub-circuit and composition-cell simulation.

Name: LogMOS

Origin: Leuven
Language: MORTRAN (object code)
Machines: DEC VAX 11/7xx, VMS.

LogMOS is a MOS logic simulator which is used for the simulation of composition-cell to LSI complexity circuits.

Name: GateSim

Origin: Digital Electronics and Computing Systems, RMIT.
Language: Pascal.
Machines: Z8Ø as above.
CDC Cyber.

GateSim is a gate level event based logic timing simulator which provides logic analyser type functions for the simulation of circuits to the MSI level of complexity.

PROCESS MODELLING

The Department has access to SUPREME and MINMOS.